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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/196,185	11/20/1998	MYUNG-KOO HUR	6192.0052.AA	8847
32605	7590	04/06/2006	EXAMINER	
MACPHERSON KWOK CHEN & HEID LLP 1762 TECHNOLOGY DRIVE, SUITE 226 SAN JOSE, CA 95110			QI, ZHI QIANG	
			ART UNIT	PAPER NUMBER
			2871	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/196,185	HUR ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 06 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-3, 6-14 and 18-26 is/are pending in the application.
- 4a) Of the above claim(s) 1-3, 6-13 and 18-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14 and 21-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948)     | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

### DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 6, 2006 has been entered.

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 14 and 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,852,481 (Hwang) in view of US 5,162,933 (Kakuda et al) and JP 05241173 (Yatabe et al).

Regarding claims 14, 23-25 and 26, Hwang discloses (col.1, line 36 – col.2, line 5; Figs.1A-1D) that a conventional thin film transistor (TFT) panel comprises:

- an insulating substrate (glass substrate 10);
- gate electrode layer (11, 12) formed on the substrate (10) which is connected with gate line, gate electrode and gate pad, so as to constitute gate wire and

supplementary gate wire on the substrate (10) having gate line, gate electrode and gate pad;

- so that the gate electrode layer (11, 12) constitutes a gate wire and a supplementary gate wire such two layers structure, and the supplementary gate wire formed on the substrate sequentially with and corresponding substantially to the gate wire;
- a gate insulating layer (15) covering the gate wire (11,12);
- a semiconductor layer (17) formed on the gate insulating layer (15);
- source/drain electrodes (19) formed on the semiconductor layer (17) which is connected with data line and data pad, so as to constitute data wire on the semiconductor layer (17) having data line, data electrode and data pad;
- a passivation layer (21) formed on the data wire and the gate wire (including the gate wire and the supplementary gate wire), and having one contact hole extended to the gate pad (12) and another contact hole extended to the drain electrode (19);
- a transparent conductive layer (indium tin oxide, ITO, to form pixel electrode 22) formed on the passivation layer (21), and connected to the gate pad (12) and the data wire (source/drain electrodes) through the contact holes.

Hwang does not explicitly disclose that:

- 1) the data wire comprising two layers structure as a data wire and a supplementary data wirer;

2) the gate wire and the data wire comprise metal or metal alloy, and the supplemental gate wire and the supplementary data wire comprise metal nitride or metal alloy nitride being inert to an etchant for preventing the gate pad or the data wire from being eroded by the etchant, and at least the supplementary gate wire or the supplementary data wire comprising tungsten, chromium.

**Kakuda** discloses (col.10, line 30 – col.11, line 55 and col.7, lines 8-28; Fig.8 and Fig.4) that the gate line (13) and the data line (11), both of them, are formed by laminating layers (13a, 13b; 11a, 11b) such as MoCr<sub>x</sub> and aluminum layers (two-layer structure in which the MoCr<sub>x</sub> layer having function of supplementary gate wire and supplementary data wire and the aluminum layer having function of gate wire and data wire comprising metal) (see Fig.8, the gate wire 13a, 13b and Fig.4, the data wire 11a,11b), and such laminated layers prevents the generation of hillock and its surface remained smooth (see col.10, lines 65-68), and the thin film transistors formed on such a layer remarkably decreasing the number of shorts (see col.10, lines 63-65), and reducing the sheet resistance so as to obtain high-speed of the data line by employ such laminated wiring structure (see col.11, lines 49-55). Kakuda further teaches the chromium (Cr) and molybdenum (Mo) are refractory metal and is excellent in heat resistance having higher workability by chemical wet etching such erodent resist property, so as to be widely used as a wiring material for the thin film device (see col,7, lines 20-28). Kakuda further teaches the tungsten (W), chromium (Cr) has low electric resistance and is particularly suitable for the lines (11,13 that include the supplementary

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gate wire and the supplementary data wire) as the wiring material (see col.7, lines 8-15).

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display of Hwang with the teachings of the gate wire and the data wire using metal layer and supplementary layer of such two layers structure as taught by Kakuda, since the skilled in the art would be motivated for several advantages set forth above such as preventing the generation of hillock and higher workability by chemical wet etching such erodent resist property (see col.10, line 30 – col.11, line 55 and col.7, lines 20-28).

Hwang and Kakuda teach the invention set forth above except for the supplementary layer comprises metal nitride or metal alloy nitride and being inert to an etchant for preventing the gate pad or the data wire from being eroded by the etchant.

**Yatabe** discloses (abstract) that the material of the electrode for liquid crystal display comprising metal nitride that is a solvent-resistant layer or air permeation resistant layer. Therefore, the metal nitride has such property to resist the solvent effect and air permeation effect, i.e., being inert to an etchant. Yatabe indicates (abstract) that using such metal nitride to obtain electrode (any electrode) enables high quality display.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display of Hwang and Kakuda with the teachings of using metal nitride as the supplemental layer as taught by Yatabe, since the skilled in the art would be motivated for the metal nitride having a solvent-resistant property so as to be inert to an etchant (see abstract).

Regarding claims 21-22, Hwang discloses (col.1, line 67 – col.2, line 5; Fig.1) that a transparent conductive layer (indium tin oxide, ITO, to form pixel electrode 22) formed on the passivation layer (21), and connected to the drain electrode (19) through a contact hole; and also using such ITO (gate ITO) connected to the gate pad (12) through another contact hole (see Fig.1D).

### ***Response to Arguments***

3. Applicant's arguments filed on March.6, 2006 have been fully considered but they are not persuasive.

(1) The reference Hwang is relied on to teach (col.1, line 36 – col.2, line 5; Figs.1A-1D) the basic LCD structure, and a transparent conductive layer (ITO) formed on the passivation layer and connected to the gate pad, and the gate wire having two layers structure.

(2) The reference Kakuda is relied on to teach (col.10, line 30 – col.11, line 55 and col.7, lines 8-28; Fig.8 and Fig.4) the gate wire (13a13b such as in Fig.8) and the data wire (11a,11b such as in Fig.4) having two layers laminated structure (a main layer and a supplemental layer, in other words, gate wire and supplementary gate wire, data wire and supplementary data wire). Some references such as US 6,107,668 (Ukita) also discloses such laminated wire technique in which (col.4, lines 51-57) the tungsten nitride film (metal nitride) is highly resistive to the chemicals and suppresses the metal from the corrosion of the electrode by the etchant; also such as US 5,334,860 (Naito).

(3) The reference Yatabe is relied on to teach (abstract) the material of the electrode for liquid crystal display comprising metal nitride that is a solvent-resistant layer or air permeation resistant layer.

### ***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299.

The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Mike Qi  
Patent examiner  
March 24, 2006